01-27-05 20 IFW

PTO/SB/21 (09-04)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/809,740
Filing Date	March 24, 2004
First Named Inventor	Tsuruta, Susumu
Art Unit	2655
Examiner Name	Unassigned
Attorney Docket Number	16869P-111000US

Total Number of Pages in This Submission: 16

ENCLOSURES *(Check all that apply)*

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☒ Petition to Make Special
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) (please identify below):
  - Return Postcard
  - Five (5) cited references

Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

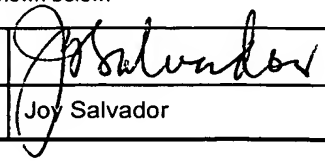
SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Townsend and Townsend and Crew LLP		
Signature			
Printed name	Chun-Pok Leung		
Date	January 25, 2005	Reg. No.	41,405

CERTIFICATE OF TRANSMISSION/MAILING

Express Mail Label: **EV 530884153 US**

I hereby certify that this correspondence is being deposited with the United States Postal Service with "Express Mail Post Office to Address" service under 37 CFR 1.10 on this date **January 25, 2005** and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature			
Typed or printed name	Joy Salvador	Date	January 25, 2005

PTO/SB/17 (12-04)

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) **130.00**

Complete if Known	
Application Number	10/809,740
Filing Date	March 24, 2004
First Named Inventor	Tsuruta, Susumu
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Art Unit	2655
Attorney Docket No.	16869P-111000US

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 20-1430 Deposit Account Name: Townsend and Townsend and Crew LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	-20 or HP =	Extra Claims	x Fee ($)	= Fee Paid ($)
_____		_____	_____	_____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	-3 or HP =	Extra Claims	x Fee ($)	= Fee Paid ($)
_____		_____	_____	_____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

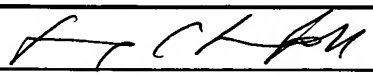
If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	- 100 =	Extra Sheets	/ 50 =	Number of each additional 50 or fraction thereof (round **up** to a whole number)	x Fee ($)	= Fee Paid ($)
_____		_____		_____	_____	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: **Petitions to the Commissioner**	**130.00**

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 41,405	Telephone 650-326-2400
Name (Print/Type)	Chun-Pok Leung		Date January 25, 2005

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PATENT
Attorney Docket No.: 16869P-111000US
Client Ref. No.: 340301295US01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: SUSUMU TSURUTA Application No.: 10/809,740 Filed: March 24, 2004 For: STORAGE CONTROL DEVICE Customer No.: 20350	Examiner: Unassigned Technology Center/Art Unit: 2655 Confirmation No.: 8162 **PETITION TO MAKE SPECIAL FOR NEW APPLICATION UNDER M.P.E.P. § 708.02, VIII & 37 C.F.R. § 1.102(d)**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a petition to make special the above-identified application under MPEP § 708.02, VIII & 37 C.F.R. § 1.102(d). The application has not received any examination by an Examiner.

(a) The Commissioner is authorized to charge the petition fee of $130 under 37 C.F.R. § 1.17(i) and any other fees associated with this paper to Deposit Account 20-1430.

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(b) All the claims are believed to be directed to a single invention. If the Office determines that all the claims presented are not obviously directed to a single invention, then Applicants will make an election without traverse as a prerequisite to the grant of special status.

(c) Pre-examination searches were made of U.S. issued patents, including a classification search, a computer database search, and a keyword search. The searches were performed on or around September 10, 2004, and were conducted by a professional search firm, Kramer & Amado, P.C. The classification search covered Class 710 (subclasses 5 and 36) and Class 711 (subclass 114) for the U.S. and foreign subclasses identified above. The computer database search was conducted on the USPTO systems EAST and WEST. The keyword search was conducted in Class 711 (subclasses 112, 113, 118, 144, 145, 162, and 168) and Class 714 (subclasses 5, 6, and 7). A literature search was conducted on the Internet for relevant non-patent documents and foreign patent documents on the Espacenet and Delphion databases. The inventors further provided one reference considered most closely related to the subject matter of the present application (see reference #5 below), which was cited in the Information Disclosure Statements filed on March 24, 2004.

(d) The following references, copies of which are attached herewith, are deemed most closely related to the subject matter encompassed by the claims:

(1) U.S. Patent Publication No. 2004/0153721 A1;

(2) U.S. Patent Publication No. 2004/0148329 A1;

(3) U.S. Patent Publication No. 2002/0124140 A1;

(4) U.S. Patent Publication No. 2004/0123028 A1; and

(5) U.S. Patent No. 5,920,893.

(e) Set forth below is a detailed discussion of references which points out with particularity how the claimed subject matter is distinguishable over the references.

A. Claimed Embodiments of the Present Invention

The claimed embodiments relate to a storage control device having a plurality of channel control sections for receiving data input and output requests from an information processing device and transmitting data to and receiving data from the information processing device.

Independent claim 1 recites a storage control device comprising a first channel control section for receiving data input and output requests from a first information processing device, and transmitting and receiving data, to and from the first information processing device; a second channel control section for receiving data input and output requests from a second information processing device, and transmitting and receiving data, to and from the second information processing device; a disk control section for reading and writing data, from and to a storage volume storing data, in accordance with the data input and output requests; and a cache memory for storing data transmitted and received between the first channel control section, the second channel control section and the disk control section. The first channel control section comprises a first memory; a first input/output control section for receiving data input and output requests from the first information processing device and controlling transmission and reception of data between the first memory and the first information processing device; a first processor for controlling the first memory and the cache memory; and a first data transfer device having a first memory controller for reading and writing data from and to the first memory, and a first data transfer control section for controlling data transfer between the first memory and the cache memory. The second channel control section comprises a second memory; a second input/output control section for controlling the second memory, receiving data input and output requests from the second information processing device and controlling transmission and reception of data between the second memory and the second information processing device; a second processor for controlling the cache memory; and a second data transfer device having a second memory controller for reading and writing data from and to the second memory, and a second data transfer control section for controlling data transfer between the second memory and the cache memory. In the first channel control section, in cases where the data input or output request received by the first input/output control section from the first information processing device is a first data write request, the first input/output control section transmits the first data

write request to the first processor; the first processor transmits first storage position information containing information indicating a storage position in the first memory for the first write data transmitted by the first information processing device, to the first input/output control section; the first input/output control section starts to transmit information indicating the storage position in the first memory for the first write data, and the first write data, to the first memory controller; the first memory controller starts to write the first write data into the first memory; the first processor transmits first data transfer information containing information indicating the storage position in the first memory of the first write data, and information indicating a storage position in the cache memory for the first write data, to the first data transfer control section; the first data transfer control section transmits a read request for the first write data written to the first memory, to the first memory controller, on the basis of the first data transfer information; the first memory controller starts to read out the first write data from the first memory; and the first data transfer control section starts to transfer the first write data read out from the first memory, to the cache memory. In the second channel control section, in cases where the data input and output request received by the second input/output control section from the second information processing device is a second data write request, the second input/output control section starts to transmit information indicating a storage position in the second memory for the second write data transmitted by the second information processing device, and the second write data, to the second memory controller; the second memory controller starts to write the second write data into the second memory; the second input/output control section transmits second storage position information containing information indicating the storage position in the second memory for the second write data, to the second processor; the second processor transmits second data transfer information containing information indicating the storage position in the second memory of the second write data, and information indicating a storage position in the cache memory for the second write data, to the second data transfer control section; the second data transfer control section transmits a read request for the second write data written to the second memory, to the second memory controller, on the basis of the second data transfer information; the second memory controller starts to read out the second write data from the second memory; and the second data transfer control section starts to transfer the second write data read out from the second memory, to the cache memory.

Independent claim 7 recites a storage control device comprising a channel control section for receiving data input and output requests from an information processing device, and transmitting and receiving data, to and from the information processing device; a disk control section for reading and writing data, from and to a storage volume storing data, in accordance with the data input and output requests; and a cache memory for storing data transmitted and received between the channel control section and the disk control section. The channel control section comprises a memory; an input/output control section for receiving data input and output requests from the information processing device and controlling transmission and reception of data between the memory and the information processing device; a processor for controlling the memory and the cache memory; and a data transfer device having a memory controller for reading and writing data from and to the memory, and a plurality of data transfer control sections for controlling the transfer of data between the memory and the cache memory. In cases where the input/output control section has received a first data write request and a second data write request from the information processing device; the input/output control section transmits the first data write request to the processor; the input/output control section transmits the second data write request to the processor; the processor transmits first storage position information containing information indicating a storage position in the memory for the first write data corresponding to the first data write request transmitted by the information processing device, and second storage position information containing information indicating a storage position in the memory for the second write data corresponding to the second data write request transmitted by the information processing device, to the input/output control section; the input/output control section starts to transmit information indicating the storage position in the memory for the first write data, and the first write data, to the memory controller; the memory controller starts to write the first write data into the memory; the processor transmits first data transfer information containing information indicating the storage position in the memory of the first write data, and information indicating a storage position in the cache memory for the first write data, to a first of the data transfer control sections; the first data transfer control section transmits a read request for the first write data written to the memory, to the memory controller, on the basis of the first data transfer information; the memory controller starts to read out the first write data from the memory; the first data transfer control section starts to transfer the first write data read out from the memory, to the cache memory; the input/output

control section starts to transmit information indicating the storage position in the memory for the second write data, and the second write data, to the memory controller; the memory controller starts to write the second write data into the memory; the processor transmits second data transfer information containing information indicating the storage position in the memory of the second write data, and information indicating a storage position in the cache memory for the second write data, to a second of the data transfer control sections; the second data transfer control section transmits a read request for the second write data written to the memory, to the memory controller, on the basis of the second data transfer information; the memory controller starts to read out the second write data from the memory; and the second data transfer control section starts to transfer the second write data read out from the memory, to the cache memory.

Independent claim 9 recites a storage control device comprising a first channel control section for receiving data input and output requests from a first information processing device, and transmitting and receiving data, to and from the first information processing device; a second channel control section for receiving data input and output requests from a second information processing device, and transmitting and receiving data, to and from the second information processing device; a disk control section for reading and writing data, from and to a storage volume storing data, in accordance with the data input and output requests; and a cache memory for storing data transmitted and received between the first channel control section, the second channel control section and the disk control section. The first channel control section comprises a first memory; a first input/output control section for receiving data input and output requests from the first information processing device and controlling transmission and reception of data between the first memory and the first information processing device; a first processor for controlling the first memory and the cache memory; and a first data transfer device having a first memory controller for reading and writing data from and to the first memory, and a plurality of first data transfer control sections for controlling data transfer between the first memory and the cache memory. The second channel control section comprises a second memory; a second input/output control section for controlling the second memory, receiving data input and output requests from the second information processing device and controlling transmission and reception of data between the second memory and the second information processing device; a second

processor for controlling the cache memory; and a second data transfer device having a second memory controller for reading and writing data from and to the second memory, and a second data transfer control section for controlling data transfer between the second memory and the cache memory. In the first channel control section, in cases where the first input/output control section has received a first data write request and a second data write request from the first information processing device, the first input/output control section transmits the first data write request to the first processor; the first input/output control section transmits the second data write request to the first processor; the first processor transmits first storage position information containing information indicating a storage position in the first memory for the first write data corresponding to the first data write request transmitted by the first information processing device, and second storage position information containing information indicating a storage position in the first memory for the second write data corresponding to the second data write request transmitted by the first information processing device, to the first input/output control section; the first input/output control section starts to transmit information indicating the storage position in the first memory for the first write data, and the first write data, to the first memory controller; the first memory controller starts to write the first write data into the first memory; the first processor transmits first data transfer information containing information indicating the storage position in the first memory of the first write data, and information indicating a storage position in the cache memory for the first write data, to any one of the first data transfer control sections; the first data transfer control section, to which the first data transfer information has been transmitted, transmits a read request for the first write data written to the first memory, to the first memory controller, on the basis of the first data transfer information; the first memory controller starts to read out the first write data from the first memory; the first data transfer control section, to which the first data transfer information was transmitted, starts to transfer the first write data read out from the first memory, to the cache memory; the first input/output control section starts to transmit information indicating the storage position in the first memory for the second write data, and the second write data, to the first memory controller; the first memory controller starts to write the second write data into the first memory; the first processor transmits second data transfer information containing information indicating the storage position in the first memory of the second write data, and information indicating a storage position in the cache memory for the second write

data, to another of the first data transfer control sections which is different to the first data transfer control section to which the first data transfer information was transmitted; the first data transfer control section, to which the second data transfer information has been transmitted, transmits a read request for the second write data written to the first memory, to the first memory controller, on the basis of the second data transfer information; the first memory controller starts to read out the second write data from the first memory; and the second data transfer control section, to which the first data transfer information was transmitted, starts to transfer the second write data read out from the first memory, to the cache memory. In the second channel control section, in cases where the data input and output request received by the second input/output control section from the second information processing device is a third data write request, the second input/output control section starts to transmit information indicating a storage position in the second memory for the third write data corresponding to the third data write request transmitted by the second information processing device, and the third write data, to the second memory controller; the second memory controller starts to write the third write data into the second memory; the second input/output control section transmits third storage position information containing information indicating the storage position in the second memory for the third write data, to the second processor; the second processor transmits third data transfer information containing information indicating the storage position in the second memory of the third write data, and information indicating a storage position in the cache memory for the third write data, to the second data transfer control section; the second data transfer control section transmits a read request for the third write data written to the second memory, to the second memory controller, on the basis of the third data transfer information; the second memory controller starts to read out the third write data from the second memory; and the second data transfer control section starts to transfer the third write data read out from the second memory, to the cache memory.

One of the benefits that may be derived is that it is capable of responding flexibly to the demands of relative cost for open information processing devices and of relative performance for mainframe information processing devices.

B. Discussion of the References

1. U.S. Patent Publication No. 2004/0153721 A1

This reference relates to a storage system including, channel control portions each including a circuit board on which a file access processing portion for receiving file-by-file data input/output requests sent from information processors through a network and an I/O processor for outputting I/O requests corresponding to the data input/output requests to storage devices are formed; disk control portions for performing data input/output of the storage devices in response to the I/O requests sent from the I/O processors; and a computer communicably connected to the channel control portions and the disk control portions. See paragraphs [0039]-[0045].

The reference discloses a storage system that includes channel control portions each including a circuit board on which a file access processing portion and an I/O processor are formed. It does not teach all the functions performed by the first channel control section in cases where the data input or output request received by the first input/output control section from the first information processing device is a first data write request, and all the functions performed by the second channel control section in cases where the data input and output request received by the second input/output control section from the second information processing device is a second data write request, as recited in claim 1. Nor does it disclose all the functions performed by channel control section in cases where the input/output control section has received a first data write request and a second data write request from the information processing device, as recited in claim 7. It further fails to teach all the functions performed by the first channel control section in cases where the first input/output control section has received a first data write request and a second data write request from the first information processing device, and al the functions performed by the second channel control section in cases where the data input and output request received by the second input/output control section from the second information processing device is a third data write request, as recited in claim 9.

2. U.S. Patent Publication No. 2004/0148329 A1

This reference discloses a storage device system capable of being connected to a plurality of different types of networks comprising, a plurality of storage devices (300) in which information is stored; a storage device control section that controls storage of information in the plurality of storage devices (300); and a connection unit connected to the storage device control section. The storage device system (600) comprises a first communication control section that includes, a first processor which is connected to the storage device control section via the connection unit and also connected on a first network external to the storage device system (600), which converts information of a first form received over the first external network into information of a second form, and which issues a request for access to the plurality of storage devices; and a second processor which accesses the plurality of storage devices (300) via the connection unit and the storage device control section in response to the access request issued from the first processor, and which controls activation of the first processor. See paragraph [0010].

The reference discloses a storage device system that includes a plurality of storage device control sections and is capable of being connected on a plurality of different types of networks. It does not teach all the functions performed by the first channel control section in cases where the data input or output request received by the first input/output control section from the first information processing device is a first data write request, and all the functions performed by the second channel control section in cases where the data input and output request received by the second input/output control section from the second information processing device is a second data write request, as recited in claim 1. Nor does it disclose all the functions performed by channel control section in cases where the input/output control section has received a first data write request and a second data write request from the information processing device, as recited in claim 7. It further fails to teach all the functions performed by the first channel control section in cases where the first input/output control section has received a first data write request and a second data write request from the first information processing device, and al the functions performed by the second channel control section in cases where the data input and output request received by the second input/output control section from the second information processing device is a third data write request, as recited in claim 9.

3. U.S. Patent Publication No. 2002/0124140 A1

This reference discloses a storage system including a storage controller. The controller (20) includes channel controllers (21), device controllers (22), a cache memory (23), and a common memory (24). The channel controller (21) is connected to a host (10) or a personal computer (PC) (40) to receive data input/output (I/O) requests from the host (10), to write data from the host (10) in a cache memory (23), and to transfer data from the cache memory (23) to the host (10). The device controller (22) writes data from the cache memory (23) in the respective storages (50, 51, 52, and 53) and transfers data from the respective storages (50, 53) to the cache memory (23). See paragraph [0025].

The reference discloses a channel controller for establishing interface for high-level devices and that, when it receives a trace information fetching indication from one of the higher-level devices, transfers the trace information to a cache memory and the storages or to the cache memory or the storages. It does not teach all the functions performed by the first channel control section in cases where the data input or output request received by the first input/output control section from the first information processing device is a first data write request, and all the functions performed by the second channel control section in cases where the data input and output request received by the second input/output control section from the second information processing device is a second data write request, as recited in claim 1. Nor does it disclose all the functions performed by channel control section in cases where the input/output control section has received a first data write request and a second data write request from the information processing device, as recited in claim 7. It further fails to teach all the functions performed by the first channel control section in cases where the first input/output control section has received a first data write request and a second data write request from the first information processing device, and al the functions performed by the second channel control section in cases where the data input and output request received by the second input/output control section from the second information processing device is a third data write request, as recited in claim 9.

4. U.S. Patent Publication No. 2004/0123028 A1

This reference relates to a storage control apparatus comprising a plurality of channel control units each having an interface with an information processor; a disk control

unit having an interface with a storage device for storing data; and a cache memory for storing temporarily data to be interchanged between the information processor and the storage device. See paragraph [0042].

The reference discloses a storage control apparatus including a plurality of channel control units each having an interface with an information processor. It does not teach all the functions performed by the first channel control section in cases where the data input or output request received by the first input/output control section from the first information processing device is a first data write request, and all the functions performed by the second channel control section in cases where the data input and output request received by the second input/output control section from the second information processing device is a second data write request, as recited in claim 1. Nor does it disclose all the functions performed by channel control section in cases where the input/output control section has received a first data write request and a second data write request from the information processing device, as recited in claim 7. It further fails to teach all the functions performed by the first channel control section in cases where the first input/output control section has received a first data write request and a second data write request from the first information processing device, and al the functions performed by the second channel control section in cases where the data input and output request received by the second input/output control section from the second information processing device is a third data write request, as recited in claim 9.

5. U.S. Patent No. 5,920,893

This reference relates to a storage control that enables data on various storage media to be shared among host computers having various different host computer input/output interfaces. A control processor checks a host computer interface management table when write is requested by a host computer (HCP). The control processor writes write data in a cache slot of the cache memory without converting the format if the data format of the HCP is in an FBA format and it converts the format into the FBA format and writes it when the data format of HCP is in a CKD format. The processor checks a table when read is requested by HCP. If the data format of HCP is FBA, the processor transfers the read data read from the cache slot without converting it and if it is CKD, the processor converts the

format into the FBA format and transfers the format converted data. The control processors, retrieve write data in the cache memory and writes it in a drive.

The reference discloses a storage control that enables various host computer input/output interfaces and/or various storage medium input/output interfaces to be added to or removed from the storage control. It does not teach all the functions performed by the first channel control section in cases where the data input or output request received by the first input/output control section from the first information processing device is a first data write request, and all the functions performed by the second channel control section in cases where the data input and output request received by the second input/output control section from the second information processing device is a second data write request, as recited in claim 1. Nor does it disclose all the functions performed by channel control section in cases where the input/output control section has received a first data write request and a second data write request from the information processing device, as recited in claim 7. It further fails to teach all the functions performed by the first channel control section in cases where the first input/output control section has received a first data write request and a second data write request from the first information processing device, and al the functions performed by the second channel control section in cases where the data input and output request received by the second input/output control section from the second information processing device is a third data write request, as recited in claim 9.

(f) In view of this petition, the Examiner is respectfully requested to issue a first Office Action at an early date.

Respectfully submitted,

Chun-Pok Leung
Reg. No. 41,405

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Attachments
RL:rl
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